

Features & Benefits

- 333 W SOSA Aligned ANSI/VITA 62.0 Compliant
- Wide Operating Temperature Range: -55 °C to 85 °C
- High Efficiency, High Power Density
- EMI Filters Included
- Up to 300 W Power on Isolated 12 V Primary Output
- Up to 33 W Power on Isolated 3.3 V Auxiliary Output
- Fixed Switching Frequency
- Droop Current Sharing & Internal ORing Diode
- Multiple Units in A Redundant or Parallel System
- IPMI 46.11 Communication
- Input Under Voltage Protection
- Input/Output Over Voltage Protection
- Short Circuit Protection
- Over Temperature Protection
- Compliant with Initial Engagement Surge from MIL-STD-1275E @333 W Output Power (Down to 10.5VDC Vin)

Compliance

Module is compliant with:

- MIL-STD-461G (CE102, CS101, CS114, CS115, CS116)
- MIL-STD-810G
- MIL-STD-1275E (All Tests)
- MIL-STD-704(A-F) ^{*(Note 1)} (All Tests)

Module is designed to meet: ^{*(Note 2)}

- CE marked
- RoHS compliant
- REACH compliant
- Def Stan 61-005
- Def Stan 00-035
- Def Stan 59-411
- Def Stan 59-114

Typical Applications

- Military/Defense Power Supplies
- Armored Vehicles
- Land Platforms
- Aerospace Platforms, Communications, and Radar Systems

| Product Ratings | |
|------------------------------|-----------|
| V _{IN} | 16 – 40 V |
| V _{OUT} (Primary) | 12 V |
| I _{OUT} (Primary) | 25 A |
| V _{OUT} (Auxiliary) | 3.3 V |
| I _{OUT} (Auxiliary) | 10 A |
| P _{OUT} (Total) | 333 W |

Product Description

This configurable power board is designed to meet the unique and challenging environmental requirements of defense applications. This VPX Board with 3U form factor delivers up to 300W power with high efficiency.

Hi-Rel VPX power supply can operate without failure under extremely harsh conditions, which is crucial for military applications.



Size: 168 × 100 × 25.4 mm

Weight: 650±20g

Note 1: Due to the absence of a hold-up capacitor in the product, it is expected that the output power will be interrupted during power interruption tests.

Note 2: Production units will be compliant with the standards outlined in this section. Testing will be completed once the detailed specifications are clarified by the end customer. Engineering prototypes do not comply.

Electrical Characteristics

All data are obtained at nominal line and full load unless otherwise specified. (Ta = 25 °C)

| Input Characteristics | | | | | |
|--|--------------------|------|------|------|------|
| Parameters | Notes & Conditions | Min | Typ | Max | Unit |
| Non-Operating Input Voltage Range | Continuous | -1 | | 50 | V |
| Operating Input Voltage Range | | 16 | 28 | 40 | V |
| Input Under Voltage Turn-On Threshold | | 10.2 | 10.6 | 11 | V |
| Input Under Voltage Turn-Off Threshold | | 10.3 | 10.5 | 10.7 | V |
| No-Load Input Current | | | 0.6 | 1 | A |
| Disabled Input Current | | | 0.2 | 0.6 | A |
| Maximum Input Current | | | 42 | | A |

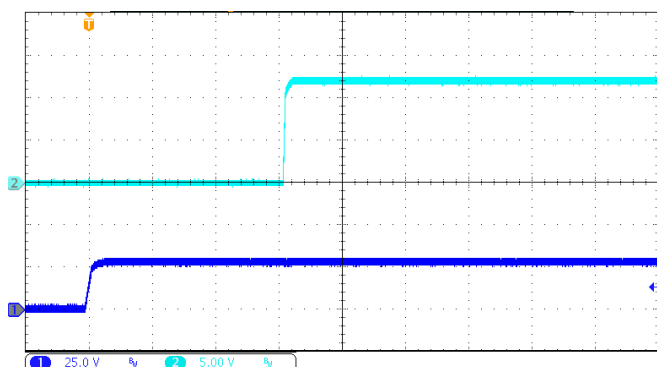
| Main Output: +12V | | | | | |
|--|---------------------------------|------|-------|------|------|
| Parameters | Notes & Conditions | Min | Typ | Max | Unit |
| Output Voltage | | 11.7 | 12 | 12.3 | V |
| Output Voltage Line Regulation | | | ± 0.1 | | % |
| Output Voltage Load Regulation | | | ± 5 | | % |
| Output Voltage Ripple and Noise (pk-to-pk) | 20 MHz bandwidth | | 35 | | mV |
| Operating Output Current Range | | 0 | | 25 | A |
| Output Current Limit | | 27.5 | | | A |
| Output Current Shutdown Limit | | | 27.5 | | A |
| Output DC Current-Limit Shutdown Voltage | | | 6 | | V |
| Output Power | | | 300 | | W |
| Output Over-Voltage Protection | At nominal output voltage | | 14.4 | | V |
| Maximum Output Capacitance | At nominal output voltage | | | 2.35 | mF |
| Input Voltage Transient Response | 50V/ms; See | | | | |
| Step Change | 18V to 36V to 18V input voltage | | 2.5 | | V |
| Settling Time | Within 1% of output voltage | | 10 | | ms |
| Load Current Transient Response | 1A/μs; See | | | | |
| Step Change | 50% to 75% to 50% output load | | 0.2 | | V |
| Settling Time | Within 1% of output voltage | | 2 | | ms |
| Turn-On Transient Time | Within 90% of output voltage | | 120 | | ms |
| Soft Start Time | Within 90% of output voltage | | 5 | | ms |

| Aux Output: +3.3V | | | | | |
|--|---------------------------------|-----|-------|------|------|
| Parameters | Notes & Conditions | Min | Typ | Max | Unit |
| Output Voltage | | 3.2 | 3.3 | 3.5 | V |
| Output Voltage Line Regulation | | | ± 0.2 | | % |
| Output Voltage Load Regulation | | | ± 1 | | % |
| Output Voltage Ripple and Noise (pk-to-pk) | 20 MHz bandwidth | | 20 | | mV |
| Operating Output Current Range | | 0 | | 10 | A |
| Output Current Limit | | 15 | | | A |
| Output Current Shutdown Limit | | | 16 | | A |
| Output Power | | | 33 | | W |
| Maximum Output Capacitance | At nominal output voltage | | | 2.35 | mF |
| Input Voltage Transient Response | 50V/ms; See | | | | |
| Step Change | 18V to 36V to 18V input voltage | | 20 | | mV |
| Settling Time | Within 1% of output voltage | | 1 | | ms |
| Load Current Transient Response | 1A/μs; See | | | | |
| Step Change | 50% to 75% to 50% output load | | 100 | | mV |
| Settling Time | Within 1% of output voltage | | 40 | | μs |
| Turn-On Transient Time | Within 90% of output voltage | | 120 | | ms |
| Soft Start Time | Within 90% of output voltage | | 5 | | ms |

| General Characteristics | | | | | |
|-------------------------|------------------------------------|-----|-----|-----|------|
| Parameters | Notes & Conditions | Min | Typ | Max | Unit |
| Efficiency | Nominal line, 50% aggregate loads | | 84 | | % |
| Efficiency | Nominal line, 100% aggregate loads | | 88 | | % |

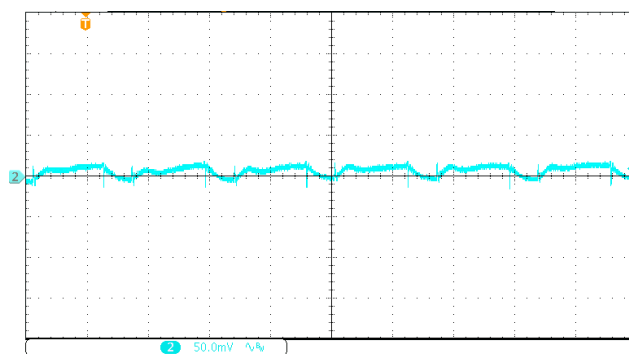
Environmental Characteristics

| Environmental Characteristics | | | | | |
|---|--|-----|-----|------|------|
| Parameters | Standard | Min | Typ | Max | Unit |
| Operational Temperature (@wedgeloek, card edge) | MIL-STD-810G_CHG-1 Method 501.6/502.6 Procedure II | -55 | - | +85 | °C |
| Storage Temperature | MIL-STD-810G_CHG-1 Method 501.6/502.6 Procedure I | -65 | - | +125 | °C |



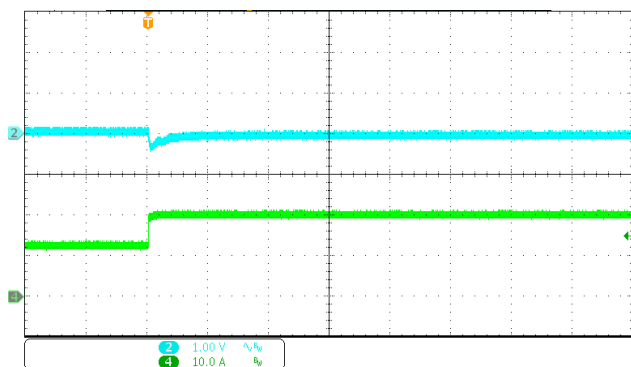
Main output voltage (navy blue) (5 V/div) Time base: 40 ms/div
Input voltage (blue) (25 V/div)

Figure A. Startup waveform of main output at full load



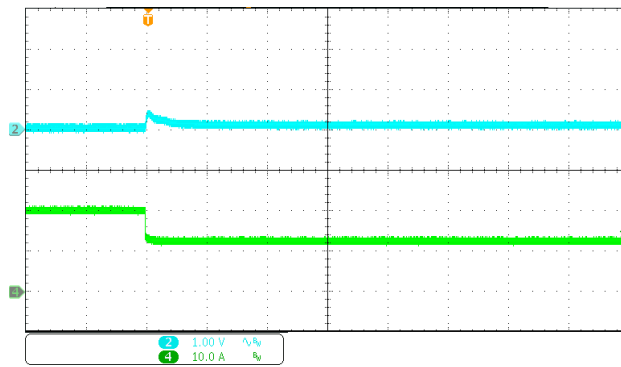
Main output voltage ripple (blue) (50 mV/div) Time base: 2 μs/div

Figure D. Main output voltage ripple at nominal input voltage and full load current



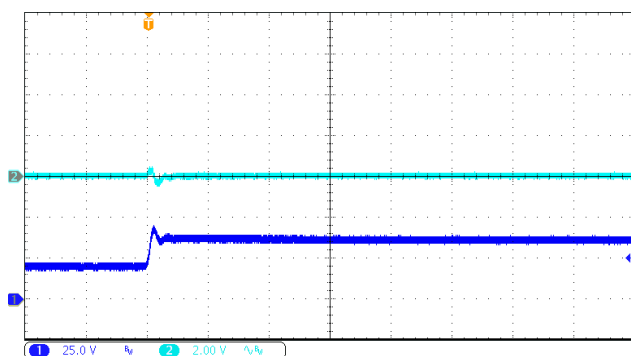
Main output voltage (blue) (1 V/div) Time base: 2 ms/div
Output current (green) (10 A/div)

Figure B. Main output load current transient response: from 50% to 75% ($di/dt = 1A/\mu s$)



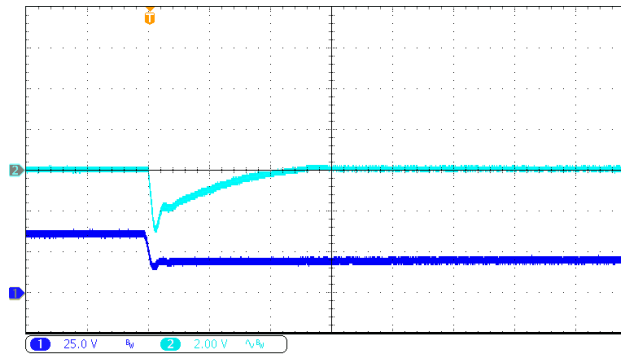
Main output voltage (blue) (1 V/div) Time base: 4 ms/div
Output current (green) (10 A/div)

Figure E. Main output load current transient response: from 75% to 50% ($di/dt = 1A/\mu s$)



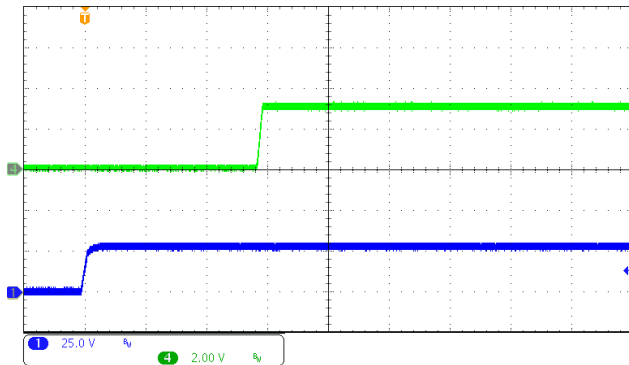
Main output voltage (blue) (2 V/div) Time base: 4 ms/div
Input voltage (navy blue) (25 V/div)

Figure C. Input voltage transient response, main output voltage (AC coupled): input voltage from 18V to 36V ($dV/dt = 50V/ms$)



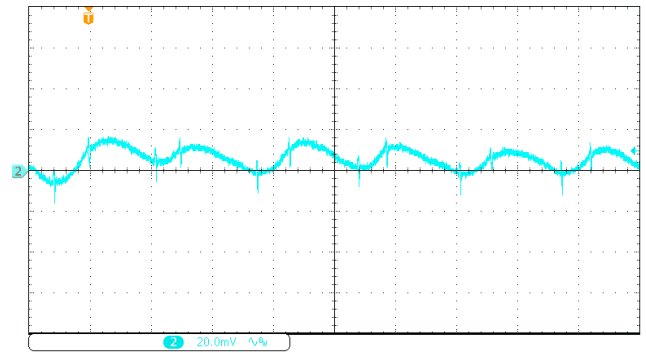
Main output voltage (blue) (2 V/div) Time base: 4 ms/div
Input voltage (navy blue) (25 V/div)

Figure F. Input voltage transient response, main output voltage (AC coupled): input voltage from 36V to 18V ($dV/dt = 50V/ms$)



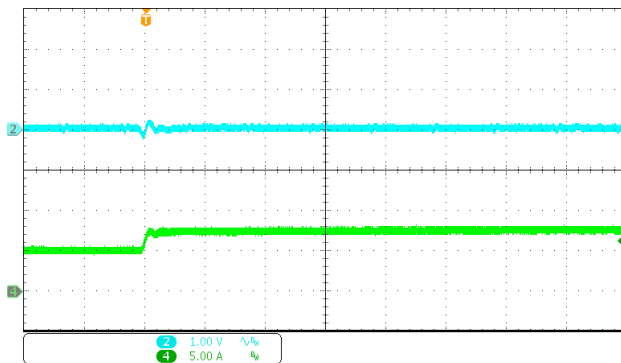
Aux output voltage (navy blue) (2 V/div) Time base: 40 ms/div
Input voltage (blue) (25 V/div)

Figure G. Startup waveform of main output at full load



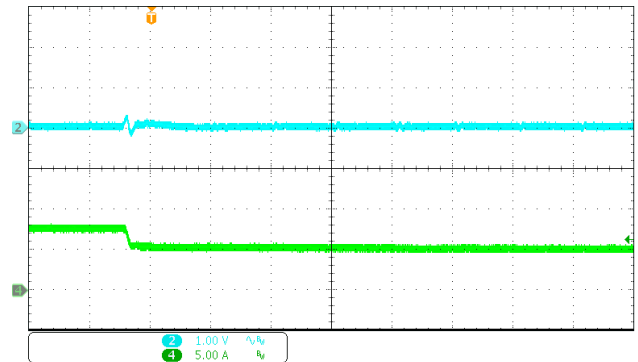
Aux output voltage ripple (blue) (20 mV/div) Time base: 2 μs /div

Figure J. Main output voltage ripple at nominal input voltage and full load current



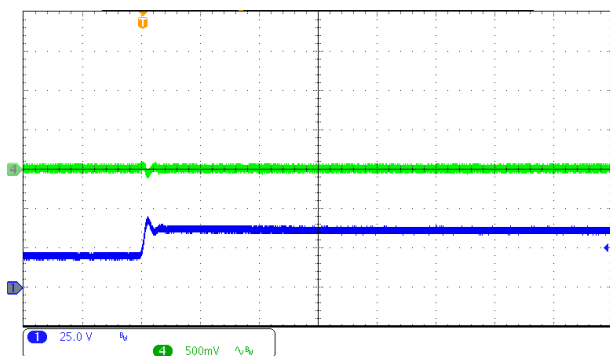
Aux output voltage (blue) (1 V/div) Time base: 40 μs/div
Output current (green) (5 A/div)

Figure H. Main output load current transient response: from 50% to 75% ($di/dt = 1A/\mu s$)



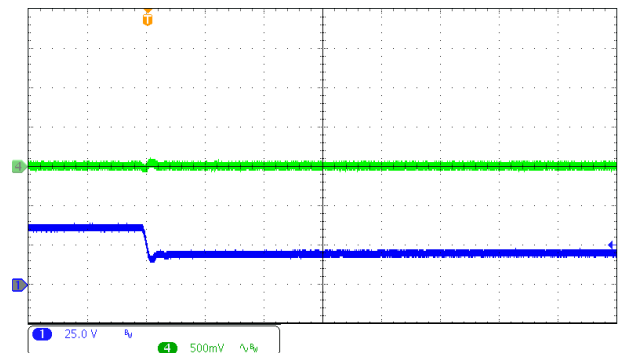
Aux output voltage (blue) (1 V/div) Time base: 40 μs/div
Output current (green) (5 A/div)

Figure K. Main output load current transient response: from 75% to 75% ($di/dt = 1A/\mu s$)



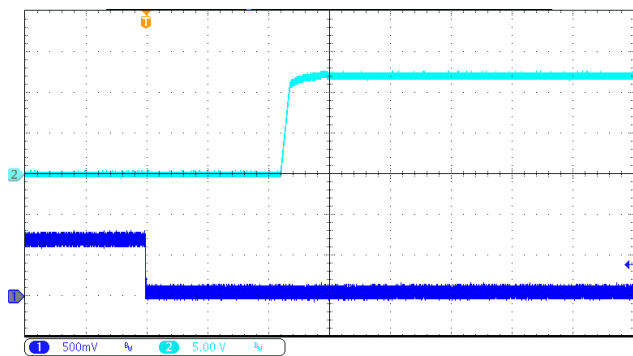
Aux output voltage (blue) (500 mV/div) Time base: 4 ms/div
Input voltage (navy blue) (25 V/div)

Figure I. Input voltage transient response, main output voltage (AC coupled): input voltage from 18V to 28V ($dV/dt = 50V/ms$)



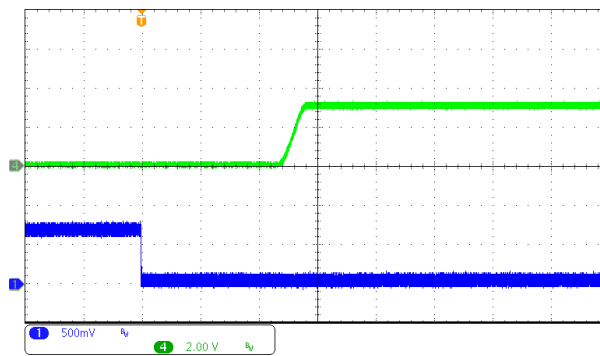
Aux output voltage (blue) (500 mV/div) Time base: 4 ms/div
Input voltage (navy blue) (25 V/div)

Figure L. Input voltage transient response, main output voltage (AC coupled): input voltage from 28V to 18V ($dV/dt = 50V/ms$)



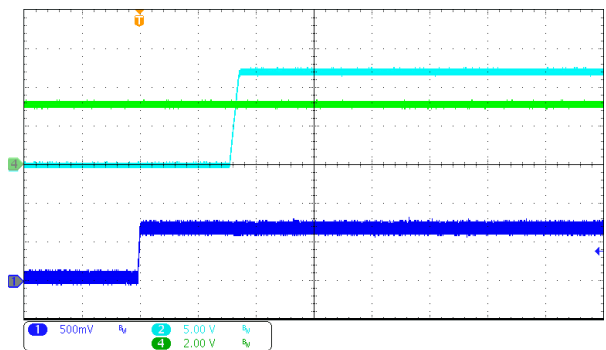
Main output voltage (blue) (5 V/div)
ENABLE* (navy blue) (500 mV/div) Time base: 10 ms/div

Figure M. ENABLE* signal asserted low



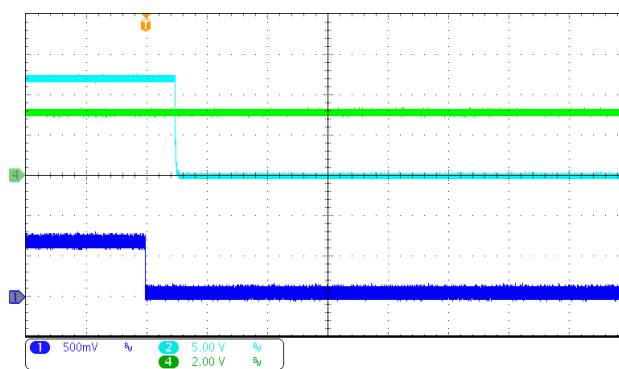
Aux output voltage (green) (2 V/div)
ENABLE* (navy blue) (500 mV/div) Time base: 10 ms /div

Figure P. ENABLE* signal asserted low



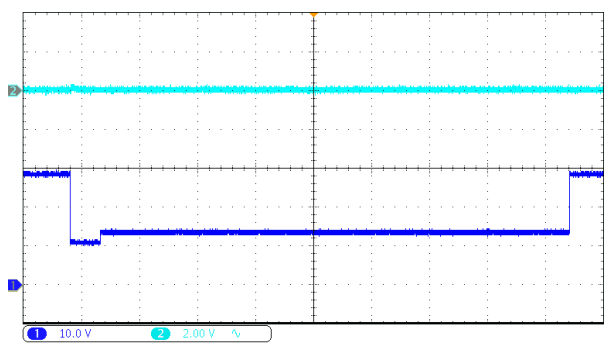
Main output voltage (blue) (5 V/div)
Aux output voltage (green) (2 V/div)
INHIBIT* signal (navy blue) (500 mV/div) Time base: 10 ms/div

Figure N. INHIBIT* asserted float



Main output voltage (blue) (5 V/div)
Aux output voltage (green) (2 V/div)
INHIBIT* signal (navy blue) (500 mV/div) Time base: 10 ms/div

Figure Q. INHIBIT* asserted low



Main output voltage (blue) (2 V/div)
Input voltage (navy blue) (10 V/div) Time base: 4 s/div

Figure O. Starting Operation Test MIL-STD-1275

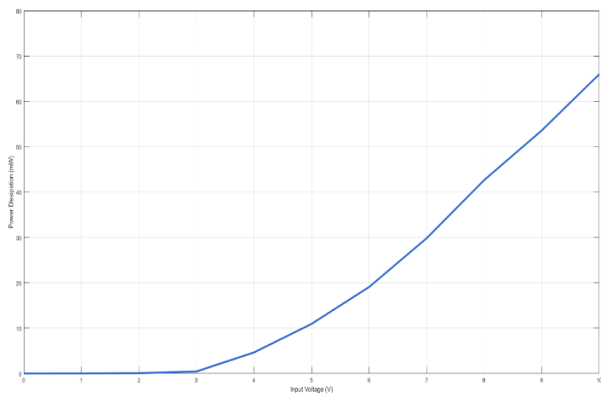


Figure R. Disabled power dissipation versus input voltage, ENABLE* asserted and INHIBT* de-asserted

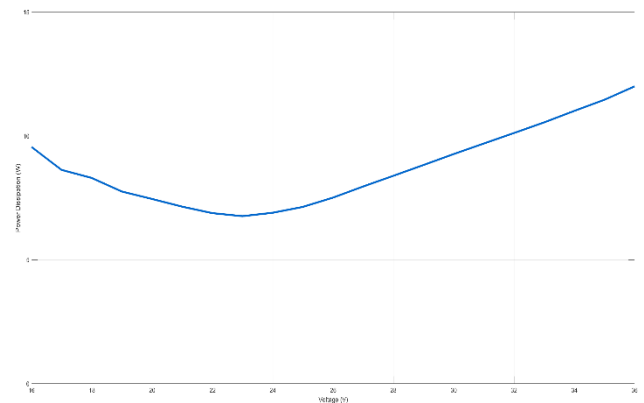


Figure T. Enabled power dissipation versus input voltage, ENABLE* asserted and INHIBT* de-asserted

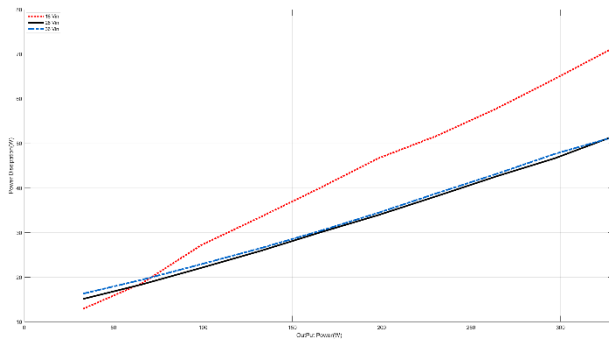


Figure S. Power dissipation versus output power at minimum, nominal, and maximum input voltage

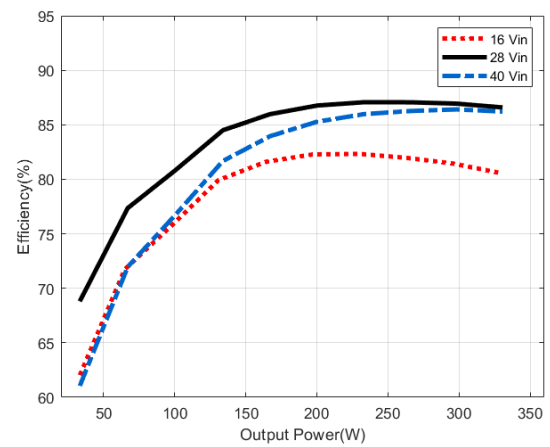


Figure U. Efficiency versus output power at minimum, nominal, and maximum input voltage

Block Diagram for KRPS02-DC28WE-P300-DC12-VX3U

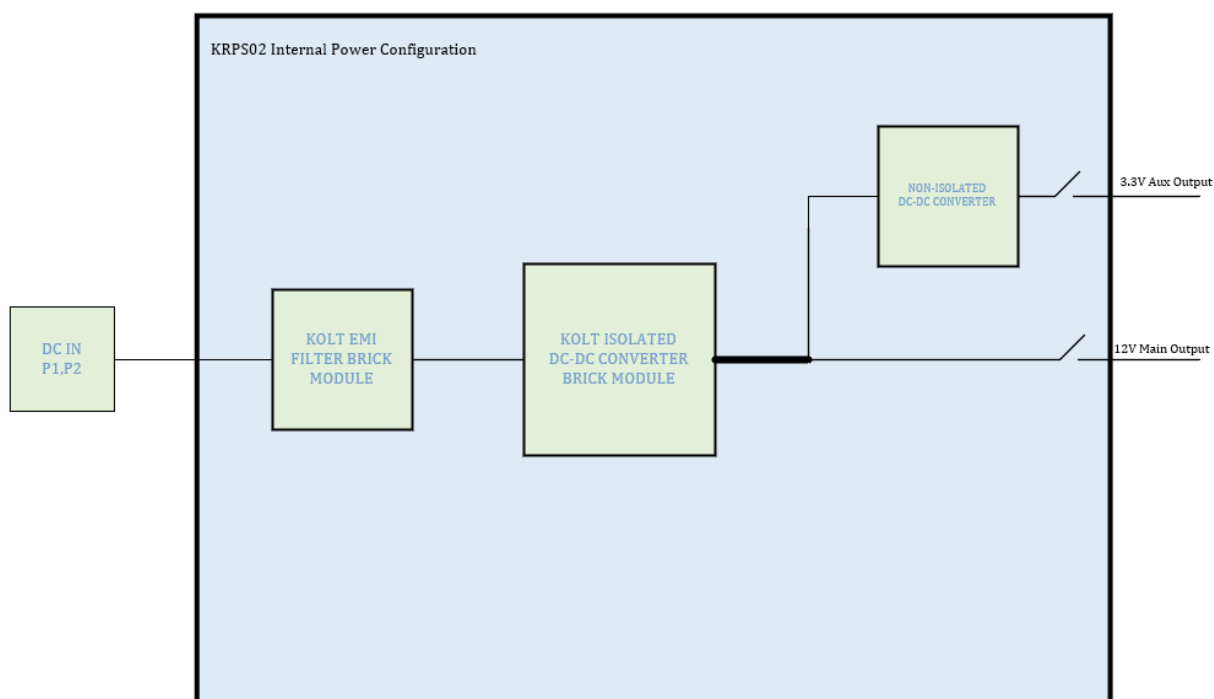


Figure V. Internal Block Diagram Representation of KRPS02

IPMI Interface

Four constants are used to calculate a real-world value from the single byte variable returned in the response. The conversions can be realized with the following equation:

$$y = (Mx + (B * 10^{K1})) * 10^{K2}$$

Where;

y = the converter reading

x = the raw sensor reading

M = the signed integer multiplier

B = the signed additive offset

K1 = signed exponent for constant B (sets decimal point for B)

K2 = signed result exponent (sets decimal point for y)

| Sensor Number | Hex | Sensor Name | SI Units | M | B | K1 | K2 |
|---------------|------|---------------------|----------|----|----|----|----|
| 7 | 0x07 | Input Voltage | V | 30 | 90 | 1 | -2 |
| 8 | 0x08 | Main Output Voltage | V | 20 | 90 | 2 | -3 |
| 11 | 0x0B | Aux Output Voltage | V | 10 | 20 | 2 | -3 |
| 18 | 0x12 | Temperature P6 | °K | 1 | 20 | 1 | 0 |
| 19 | 0x13 | Temperature P1 | °K | 1 | 20 | 1 | 0 |
| 25 | 0x19 | Aux Output Current | A | 10 | 0 | 0 | -2 |

Protection Features

Input Under Voltage Lockout

The VPX module starts operating when the input voltage is raised above the "Under Voltage Turn-On Threshold." Once turned on, turn off is initiated when the input falls below the "Under Voltage Turn-Off Threshold." The "Module Input Specifications" Table gives the associated limits.

Input Over Voltage Protection

The VPX module protects itself by ceasing operation when the input goes above the "Over Voltage Turn-Off Threshold." It resumes operation when the input falls below the "Over Voltage Turn-On Threshold." The associated limits are given in the "Module Input Specifications" Table.

Output Current Limit

The VPX module will derate the output voltage if the output current exceeds the "Output Current Limit" value. If the fault condition is resolved, the control output voltage will increase to the nominal value.

Output Over Voltage Protection

If the output voltage exceeds the "Output Over Voltage-Protection" value the VPX module outputs are disabled immediately and retries after cooldown period. The "Output Over Voltage Protection Limit" is 120% of Output Voltage.

Output Over Current Protection

If the output current exceeds the "Output Current Shutdown Limit" value the VPX module outputs are disabled immediately and retries after cooldown period.

Short Circuit Protection

The short circuit condition is an extreme case of the Output Current Limit condition. When output voltage drops below "Output DC Current-Limit Shutdown Voltage" limit, the VPX module outputs are disabled immediately and retries after cooldown period. The "Output DC Current-Limit Shutdown Voltage" is 50% of Output Voltage.

Over Temperature Shutdown

The brick has a thermistor located at the hottest point inside the module. The thermal shutdown circuit is designed to turn the VPX module off when the temperature at the sensed location goes above the "Over Temperature Shutdown" limit. It locks itself and waits to cool off. The VPX module then resumes operation automatically when the temperature of the sensed location falls below the trip point by the amount equal to the "Over Temperature Shutdown Hysteresis."

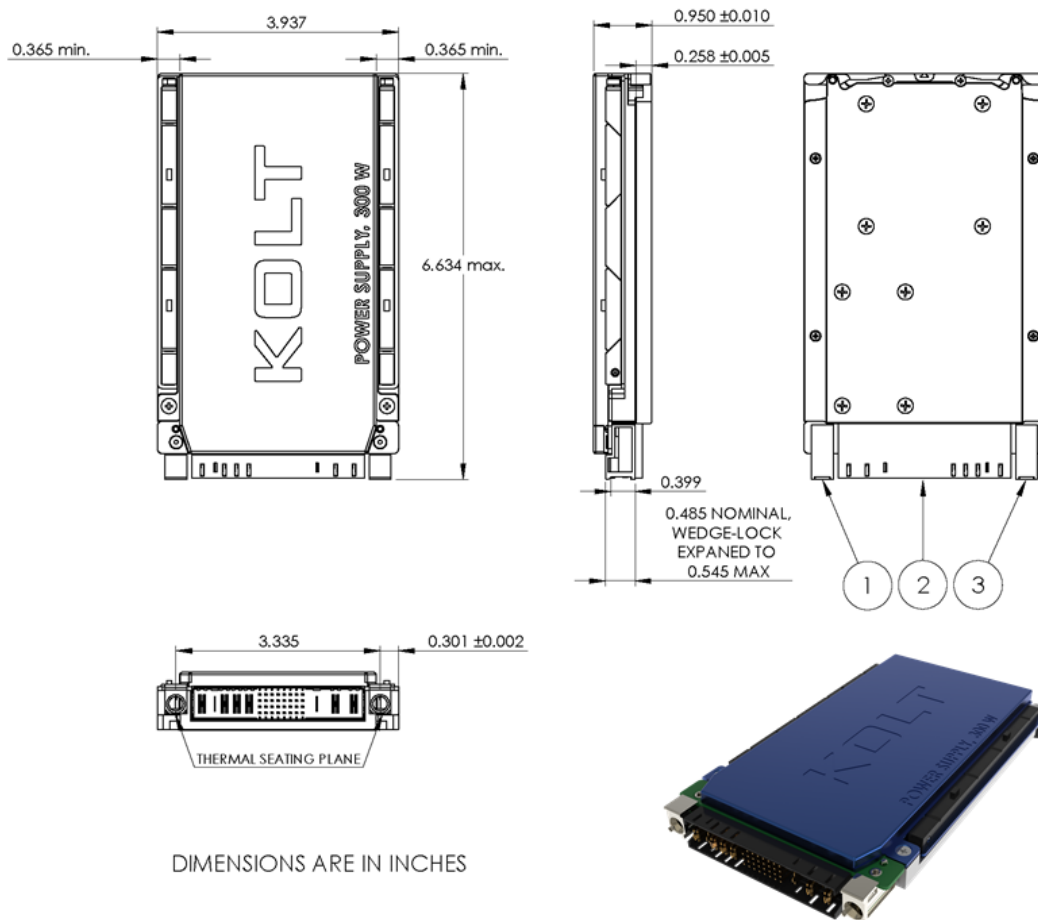
Mechanical Drawing

Connector Pin Configuration

| ROWS | POWER | | | SIGNAL | | | | | | | | POWER | | | | |
|------|-------|----|-----|--------|---|---|---|---|---|---|---|-------|----|----|-----|----|
| | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | | | | | |
| D | P1 | P2 | LP1 | | | | | | | | | P3 | P4 | P5 | LP2 | P6 |
| C | | | | | | | | | | | | | | | | |
| B | | | | | | | | | | | | | | | | |
| A | | | | | | | | | | | | | | | | |

| Pin | Function/Name | Description |
|-----|---------------------|---|
| P1 | -DC_IN | V _{in} - |
| P2 | +DC_IN | V _{in} + |
| LP1 | CHASSIS | - |
| A1 | NC (SYNC_OUT) | - |
| B1 | NC (NVMRO) | - |
| C1 | GA2* | Address Bit 2 |
| D1 | NC | - |
| A2 | NC (VBAT) | - |
| B2 | FAIL* | When any of the output is not within specification, FAIL* signal will be driven low to indicate a failure |
| C2 | INHIBIT* | Input control signal defined in VITA 62, referenced to SIGNAL RETURN |
| D2 | ENABLE* | Input control signal defined in VITA 62, referenced to SIGNAL RETURN. |
| A3 | NC (SYNC_IN) | - |
| B3 | NC | JTAG VDD |
| C3 | NC (NED) | - |
| D3 | NC (NED_RETURN) | - |
| A4 | NC | JTAG TDO |
| B4 | NC | JTAG TCK |
| C4 | NC | JTAG TDI |
| D4 | NC | JTAG TMS |
| A5 | GA0* | Address Bit 0 |
| B5 | GA1* | Address Bit 1 |
| C5 | SM0 (IPMB-A SCL) | Primary I ² C clock |
| D5 | SM1 (IPMB-A SDA) | Primary I ² C data |
| A6 | SM2 (IPMB-B SCL) | Redundant I ² C clock |
| B6 | SM3 (IPMB-B SDA) | Redundant I ² C data |
| C6 | NC | - |
| D6 | SYSRESET* | System reset is actively low. It will be high impedance when all outputs are within voltage specification. It will be pulled low if any failure has occurred or if the outputs are disabled by the user during operation. |
| A7 | NC (+12VDC SHARE) | - |
| B7 | NC (3.3V_AUX SHARE) | |
| C7 | NC (+12VDC SHARE) | |
| D7 | SIGNAL RETURN | Ground pin for control and communication signals; internally Kelvin-connected to POWER RETURN |
| A8 | +12VDC SENSE | Main output sense, should be connected at point-of-load |
| B8 | 3.3V_AUX SENSE | Aux output sense, should be connected at point-of-load |
| C8 | +12VDC SENSE | Main output sense, should be connected at point-of-load |
| D8 | SENSE RETURN | Aux output sense, should be connected at point-of-load |
| P3 | +12VDC | +12V main output |
| P4 | POWER RETURN | Common output voltage return pin |
| P5 | POWER RETURN | |
| LP2 | 3.3V_AUX | +3.3V auxiliary output |
| P6 | +12VDC | +12V main output |

Mechanical Dimensions



| Item | Description | Manufacturer Part Number | Manufacturer |
|------|----------------------------|--------------------------|-----------------|
| 1 | VITA 46 0 Deg Guide Socket | 1-1469492-1 | TE Connectivity |
| 2 | VITA 62 Connector Plug | 6450849-7 | |
| 3 | VITA 46 0 Deg Guide Socket | 1-1469492-1 | |

Part Ordering Information

| Family | Input Voltage | Power | Output Voltage | Package | Option Field |
|--------|------------------|---------------|----------------|----------------|--------------|
| KRPS02 | DC28WE 28 VDC | P300 300 W | DC12 12 VDC | VX3U 3U VPX | - |

Revision History

| Document Number | Revision | Date | Description | Page Number(s) |
|-----------------|----------|------------|---|----------------|
| 110267 | 01 | 02.04.2025 | Initial Release | - |
| 110267 | 02 | 16.05.2025 | Second Release <ul style="list-style-type: none">Electrical characteristics updatedMain and aux output measurements addedEfficiency measurements addedInternal block diagram added | All Pages |

Contact Us

KOLT Türkiye

salesturkiye@koltpower.com

KOLT Muhendislik A.S.

Serhat Mah. 1148. Sok.
No:1B/1 Yenimahalle, Ankara 06374

Türkiye

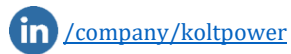
www.kolt.com.tr**KOLT Europe**

saleseurope@koltpower.com

KOLT Power Ltd.

Fareham Innovation Centre Merlin House, 4 Meteor
way,
Daedalus Drive, Fareham, Lee-On-Solent PO13 9FU

United Kingdom

www.koltpower.com

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